

What is Claimed:

- 1 1. A method for manufacturing an integrated circuit comprising: 6,251,740
2 (a) forming an opening in a layer for a dual damascene structure; and
3 (b) forming at least two openings in the layer for a capacitor.
1 2. The method of claim 1 wherein steps (a) and (b) occur at
2 substantially the same time.
1 3. The method of claim 1 wherein step (a) further comprises:
2 (a1) forming a groove; and
3 (a2) forming a via.
1 4. The method of claim 3 wherein steps (a1) and (b) occur at
2 substantially the same time.
1 5. The method of claim 3 wherein steps (a2) and (b) occur at
2 substantially the same time.
1 6. The method of claim 1 further comprising:
2 (c) filling the opening with a conductive material to form a dual
3 damascene structure; and
4 (d) filling the at least two openings with the conductive material to form
5 the capacitor.
1 7. The method of claim 6 wherein steps (c) and (d) occur at
2 substantially the same time.
1 8. The method of claim 1 wherein the layer comprises a plurality of
2 layers.
1 9. The method of claim 8 wherein the plurality of layers includes at
2 least one etch stop layer.
1 10. A method of manufacturing an integrated circuit comprising:
2 (a) forming a plurality of layers;
3 (b) partially forming a dual damascene structure by forming a first
4 opening in at least one of the plurality of layers; and

5 (c) partially forming a capacitor by forming second and third openings in
6 at least one of the plurality of layers.

1 11. The method of claim 10 wherein the first, second, and third
2 openings have substantially the same width.

1 12. The method of claim 10 wherein the second and third openings
2 have a first width and the first opening has a second width different from the first width.

1 13. An integrated circuit comprising:
2 a layer;
3 a dual damascene structure formed in the layer;
4 a capacitor formed in the layer, the capacitor having a first conductor and
5 a second conductor formed in the layer.

1 14. The integrated circuit of claim 13 wherein the layer includes at
2 least two layers.

1 15. The integrated circuit of claim 13 wherein the first conductor and
2 the second conductor are not formed above or below each other.

1 16. The integrated circuit of claim 13 wherein:
2 the layer includes a stop layer; and
3 the dual damascene structure includes at least a groove and a via where a
4 bottom portion of the groove includes at least a top portion of the stop layer.

1 17. The integrated circuit of claim 16 wherein the stop layer is formed
2 between the first conductor and the second conductor.

1 18. The integrated circuit of claim 13 wherein the layer includes a stop
2 layer and the stop layer is formed between the first conductor and the second conductor.

1 19. The integrated circuit of claim 18 wherein the first conductor and
2 the second conductor contact the stop layer.

1 20. The integrated circuit of claim 19 wherein the first conductor
2 includes a liner and a conductive material.

1 21. The integrated circuit of claim 13 wherein the first conductor is a
2 first plate of the capacitor and the second conductor forms the second plate of the
3 capacitor.

1 22. The integrated circuit of claim 13 further comprising a substrate
2 where the layer is formed on the substrate and the layer is at least not formed between the
3 first conductor and the substrate.